International Journal of Electrical and
Electronics Engineering Research (IJEEER)
ISSN(P): 2250-155X; ISSN(E): 2278-943X
Vol. 4, Issue 2, Apr 2014, 83-90

TRANS STELLAR
• Journal Publications • Research Consultancy

DESIGN OF A 4-BIT VEDIC MULTIPLIER USING TRANSISTORS

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ABSTRACT

CMOS Logical circuits are widely used in the designing of Power and area efficient multiplier in various digital signal processors. The ancient philosophy of Vedic multiplication advantage can be taken for the multiplier implementation with the help of "Urdhva Tiryak Bhyam sutra". In almost all the processors, multiplier p lays a vital role & contributes substantially to the total power consumption of the system. This is very reliable because of the use of the Vedic algorithm (sutras) that reduces the number of computational steps to a great extent compared to any conventional method. This paper presents a high performance multiplier which has the maximum power reduction compared to gate level analysis. The schematic for this multiplier is designed using CADENCE tool. The design is then simulated in ADE using spectra in 180nm CMOS technology library file.

KEYWORDS: Component, Multiplier,Vedicalgorithms, Urdhva Tiryak Bhyam Sutra

INTRODUCTION

Off late, a Multiplier is an essential block in any DSP Signal Processing & VLSI Signal Processing Applications. A binary multiplier is used in digital electronics & computer, to multiply two binary numbers. Digital Multiplier can be implemented through a variety of techniques. Most of the techniques compute a set of partial products sums them. This process is applicable for multiplication onbase-10 integers, but has been modified here for application to a base-2 (binary) number system. Due to larger integration, more transistors per chip became available which enables to put enough adders on a single chip to sum all the partial products at once, rather than reuse a single adder to handle each partial product one at a time.

Processors spend enormous amount of time & a lot of chip area on multiplying, in order to make the multiplication as fast as possible. The parallel multipliers are mainly classified as array based and tree based multipliers. The add and shift multiplier will work as normal array multiplier. A tree based multiplier called Wallace tree multiplier operates at high speed. The irregularity in structure is the main disadvantage in this multiplier. Braun Multiplier is one of the parallel array based multiplier which requires n^2 gates and (n-1) adders. So the area complexity increases with the number of bits. Baugh-Wooley multiplier is an array multiplier that can perform signed multiplication but again it has a drawback on area. So, Booth Multiplier was designed to overcome the drawback of area but it will not work when it has alternate zeros and ones and it requires more number of additions and subtractions. This problem is overcome by Modified booth multiplier, in which number of partial product rows is reduced by half.

It performs well in terms of speed and power consumption but the main disadvantage is it will not work for negative numbers. Hence a non-conventional yet very efficient Vedic mathematics is used for making a high performance multiplier. Vedic Mathematics deals mainly with various Vedic mathematical formulae and their applications for carrying out large arithmetical operations easily [9]. Vedic Mathematics was introduced by Jagadguru Swami Sri Bharati Krishna

Tirthaji Maharaja (1884-1960). Sri Sankaracharya defined Vedas as “the fountain head and illimitable store house of all knowledge”.

VEDIC MULTIPLICATION METHODS

Sutras of Vedic Multiplication

Based on various branches of mathematics, Vedic algorithms are divided into 16 sutras (Algorithms) [10], out of which two sutras are for Multiplication as:

- Nikhilam Navatashcaramam Dashatah – All from 9 and the last from 10.
- Urdhva-Tiryak Bhyam – Vertically and Crosswise.

Nikhilam sutra is not a generalized multiplication approach. So it is better to employUrdhvaTiryakBhyam sutra of Vedic Multiplication which is the most generalized sutra for multiplication. Urdhva means vertically up-down, Tiryak Bhyam means left to right or vice versa.

This paper focuses the technique which is used for binary multiplication for making the digital multiplier. It can also be called as Vertically and Crosswise” method of multiplication. An illustration of this multiplication algorithm is shown in the figure below. This algorithm considers a digital hardware because of which the Vedic Multiplier will be more power efficient and quick as less number of steps is required for multiplication having hardly any limitation attached to it [1]

Urdhva Tiryagbhyam Sutra

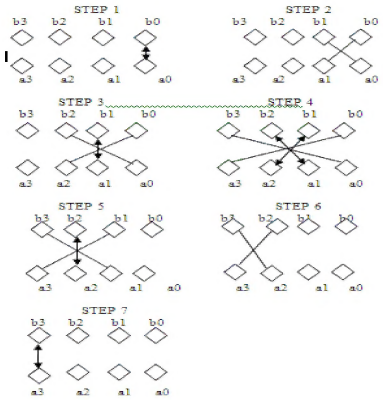


Figure 1: Line-Diagram for Urdhva-Tiryagbhyam Sutra of Multiplication

Above figure clearly depicts the generalized line-diagram structure of the Urdhva-Tiryakbhyam algorithm This algorithm maybe applied even in the case of division of two numbers [10]. The multiplication process here are in vertical and crosswise directions, requiring only 7 steps for multiplication of two, 4 bit numbers.

The advantages of Vedic Multiplier are:

- It provides effective algorithms used in various branches of engineering such as computing.
- It is very simple as it is based on natural principles on which human brain works.
- It reduces the number of computational steps to a considerable extent compared to conventional mathematics.
- It is used in higher order multiplication because it has been modified & developed for best efficiency.

- It is used in high speed DSP, VLSI Signal Processing Applications because of its high speed.
- The area occupied by the multiplier reduces as the number of transistors reduces.

Analog Design of Vedic multiplier employed in this paper is more efficient than the digital design as we have a provision to design our own library which is not possible in digital design where the libraries are inbuilt which sometimes uses larger number of transistors.

This paper composed of the schematics and simulation results of 14 transistor adder, 2 I/P AND gate & a 4-bit Vedic Multiplier.

RELATED WORKS

Various papers explain different approaches of multiplication. In some multipliers, processors become independent of clock frequency [2]. This is due to the involvement of parallelism approach where the multiplier will require the same amount of time to calculate the partial product & their sums and hence is independent of the clock frequency. Vedic Mathematics helped in the evolution of high speed multiplier design (ASIC) presented in [3] where the carry propagation is reduced from LSB to MSB by generating the partial products & their sums in a single step. Usage of Vedic Algorithms in DSP is focused in [4]. Here the Implementation on 8085 and 8086 microprocessors using Vedic mathematics is shown where an appreciable saving of processor's time is seen. Vedic Mathematics was also helpful in conserving the area, time, power of a multiplier in [5]. Here a comparison between various multipliers is done and conclusion is made that booth and array multipliers are faster among the conventional multipliers.

Digital arithmetic developed using reduced bit multiplication algorithm is shown in [6]. Here Urdhvatiryakbhyam sutra &Nikhilam sutra are explained in detail where two 8bit no's are split into four 4 bit numbers & then multiplied. To show that Vedic square and cube architecture were faster than the conventional square and cube architectures, a novel design for square and cube architecture was shown in [7]. The fundamental of any Vedic mathematics based calculations right from scratch is shown in [8]. This contains the complete essence of the Vedic techniques, sutra explanations and complete discussions with all the explanations given in detail enabling even a common man to understand these formulae without any difficulty.

PROPOSED WORK

Concept of Vedic Multiplier

Vedic mathematics is an extract from four Vedas (books of wisdom). It is actually a sub module of Sthapatya-veda (book on civil engineering and architecture), which is an upya-veda (supplement) of Atharva Veda.

In this 4 bit Vedic multiplier approach, considering the line diagram & considering the schematic, the LSB bit of both the operands are first multiplied & the partial product is noted in the first step i.e., a0, b0 are multiplied using the and gate & the LSB is obtained. The last two bits of both the operands are multiplied in a crosswise direction i.e., a1 b0, a0 b1 are multiplied using two separate AND gates (Figure 3) and the product of these two AND gates are fed to the 14T full adder (Figure 2) to obtain the next bit. Now the last three bits of both operands as shown in line diagram (Figure 1) are multiplied in a vertically crosswise direction using 3 AND gates whose outputs are fed to full adder to obtain the 3rd bit. Similarly the next four bits along with carry is generated with the help of line diagram constituting a 4 bit Vedic multiplier which is designed using transistors shown in (Figure 4)

Design of Vedic Multiplier

This paper is composed of mainly 3 designs designed using transistors in Cadence Virtuoso is discussed below.

14T Full Adder

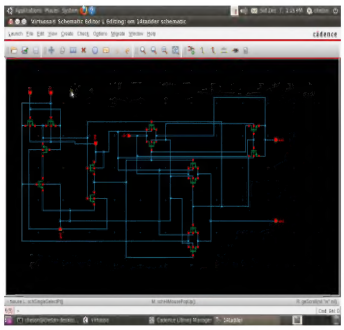


Figure 2: Schematic for 14T Full Adder in Cadence Tool

The Full Adder designed in this paper is a 14T adder based on complimentory pass-transistor logic (CPL). The schematic design is as shown in (Figure 2). The design is composed of XOR & XNOR gates combined together to make a low power Full Adder with high node voltage swings consuming low power.

The Sum & Carry outputs are generated from Binary inputs A, B, Cin & expressed as

Sum = A XOR B XOR Cin

Cout = A.B + Cin. (A XOR B).

After designing the 14T Adder it is very essential to design a AND Gate to multiply two bits at a time. The schematic of AND is as shown in Figure 3.

The 4 bit Vedic Multiplier design using a series of AND gates & Full Adders as shown in Figure 4. The inputs are a0a1a2a3 & b0b1b2b3. Design is according to the CMOS Logic.

AND Gate

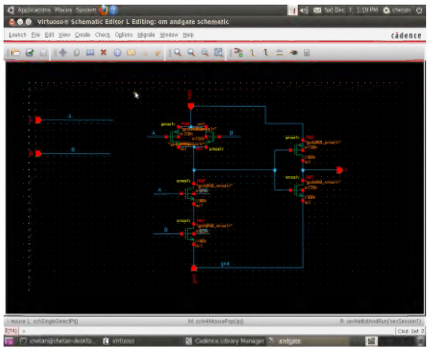


Figure 3: Schematic for AND Gate in Cadence Tool

4 Bit Vedic Multiplier

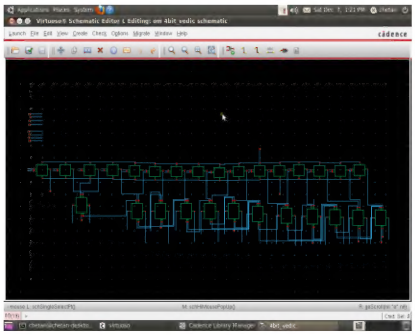


Figure 4: Schematic for 4 Bit Vedic Multiplier in Cadence Tool

The only limitation with this multiplier is, for complex multiplications, the system becomes too complex but that does not affect the performance or speed as we use Binary numbers. As the multiplier is using large number of MOSFETS, buffers will be required at various nodes inside the circuit for avoiding the voltage drop inside the circuit[11]. So the circuit becomes bulkier. This design can be further optimised by using less number of transistors for the full adder.

RESULT ANALYSIS

Tools Used

All the schematic designs in this paper are presented using the Cadence Virtuoso Tool. The design is then verified or simulated in Analog Design Environment through simulation using the simulator called spectra using 180nm CMOS Technology File.

Simulation Results

The output of the first schematic design shown in the paper that is 14T Full Adder is verified by the simulation waveform result shown in Figure 5.

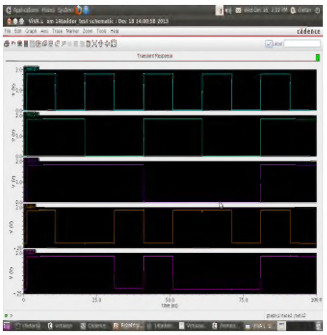


Figure 5: Output Waveform for 14T Full Adder

The design is simulated in 180nm library file and the instance is made. The output waveforms of AND Gate (Figure 6) & that of 4 bit Vedic multiplier (Figure 8) are as shown. To obtain the waveforms of 4 bit Vedic Multiplier, any two 4 bit binary numbers can be chosen. A test circuit of 4 bit Vedic multiplier is as shown in Figure 7.

In the test circuit, both of the 4 bit operands are considered as 1111, i.e, a0=a1=a2=a3=b0=b1=b2=b3=1, where a3, b3 are considered to be the MSB & a0, b0 are LSB bits.

The test circuit is shown (figure 7) showing the value of current and indicating that logic 1 is given to all the inputs. The output waveform of 4 bit Vedic multiplier is as shown in Figure 8. The Binary 1 is represented as Logic high that is 1.8V & Logic 0 is indicated in the order of few microvolts. The output will be11100001, starting from MSB to LSB.

It is shown in waveform starting from LSB, P0 to MSB P7, 8 bits in total.

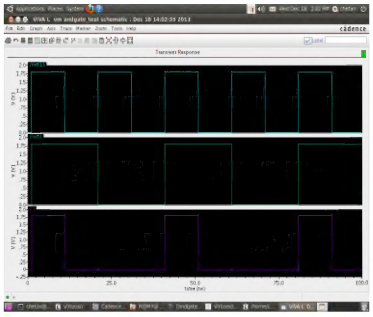


Figure 6: Output Waveform for AND Gate

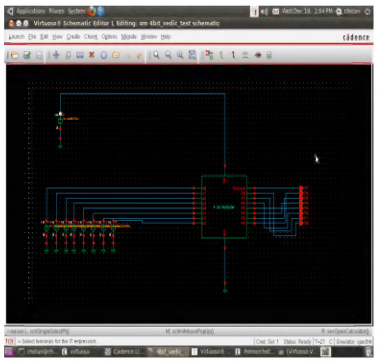


Figure 7: Test Circuit of 4 Bit Vedic Multiplier

Performance Analysis

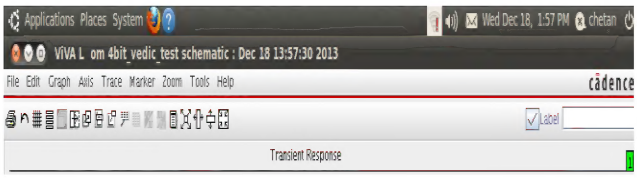
The multiplier blocks are simulated using spectra simulator and the following observations are made for 4 bit multiplier.

No of Transistors for Adder = 14T

Average Power = 17.45 uW

The conventional multiplier consists 28 transistors whereas in case of Vedic Multiplier we use very less Transistors thereby we can reduce the area, hardware required, reduce the number of computational steps leading to the enhancement in the overall performance.

If we consider the aspect of power, using gate level analysis, the power is found to be 0.45W for a 4 bit Vedic Multiplier. So it is found that the power consumption is reduced greatly.



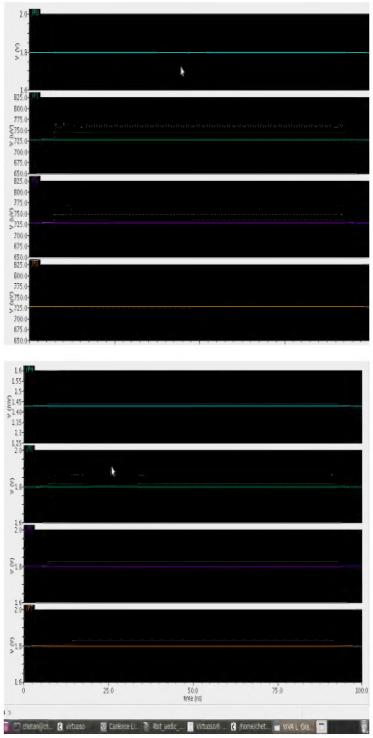


Figure 8: Output Waveforms of 4 Bit Vedic Multiplier

CONCLUSIONS

This paper represents an efficient Vedic Multiplier design using VLSI technology. We achieve almost 80% of the power reduction as compared to the other conventional ways of multiplication using Gate level Analysis, also the computational complexity is less as it requires lesser number of steps. All the circuits are implemented here in Cadence Tool. This design implementation & results show that a major step is taken in reducing the area & power when compared to conventional multipliers. This multiplier shows an improvement in power consumption & can be efficiently used in any DSP application or in any DSP processors & VLSI Signal Processing Applications that requires low power consumption [12].

ACKNOWLEDGEMENTS

Paper is a job of great enormity and it cannot be accomplished by an individual all by them. Eventually I am grateful to a number of individuals whose professional guidance, assistance and encouragement have made it pleasant endeavours to prepare this paper. I have great pleasure in expressing our deep sense attitude to our principal, Dr. Rana Pratap Reddy, Reva Institute of Technology for constant support & encouragement. I convey my regards to Dr. S.S. Manvi, Professor and HOD, Dept of ECE for having constantly monitored the development of the paper. Finally I would like to express my gratitude to my family and friends who helped me in consolidating the information related to the topic explained in the paper.

REFERENCES

1. Arun. K. Patro, Kunal. N. Dekate, “A Transistor Level Analyses for a 8 bit Vedic Mutiplier”, IJESS, vol 1 Iss-3, 2012, pp 78-83.

2. Ramachandran. S, Kirti. S. Pande, Design, Implementation & Performance Analysis of an Integrated Vedic multiplier Architecture", International Journal of Computational Engineering Research, Vol. 2, Issue No. 3, May-June 2012, pp 697-703.

3. Prabir Saha, Arindham Banerjee, Partha Battacharyya, Anup Dhandapat, "High speed design of complex multiplier using Vedic mathematics", Proceedings of the 2011 IEEE students technology symposium, IIT Kharagpur, pp. 237-241, Jan. 2011.

4. Purushottam D. Chidgupkar and Mangesh T. Karad, "The Implementation of Vedic Algorithms in Digital Signal Processing", UICEE, Global J. of Engng. Educ., Vol.8, No.2, pp. 153-158, 2004.

5. Himanshu Thapliyal and Hamid R. Arabnia, "A Time-Area- Power Efficient Multiplier and Square Architecture Based On Ancient Indian Vedic Mathematics", Department of Computer Science, The University of Georgia, 415 Graduate Studies Research Center Athens, Georgia 30602-7404, U.S.A.

6. E. Abu-Shama, M. B. Maaz, M. A. Bayoumi, "A Fast and Low Power Multiplier Architecture", The Center for Advanced Computer Studies, The University of Southwestern Louisiana Lafayette, LA 70504.

7. Himanshu Thapliyal, Saurabh Kotiyal and M. B Srinivas, "Design and Analysis of A Novel Parallel Square and Cube Architecture Based On Ancient Indian Vedic Mathematics", Centre for VLSI and Embedded System Technologies, International Institute of Information Technology, Hyderabad, 500019, India, 2005 IEEE.

8. Jagadguru Swami Sri Bharati Krishna Tirthji Maharaja, "Vedic Mathematics", Motilal Banarsidas, Varanasi, India, 1986.

9. Honey Durga Tiwari, Ganzorig Gankhuyag, Chan Mo Kim, Yong Beom Cho, "Multiplier Design based on ancient Indian Vedic Mathematics", 2008 International SoC Design Conference.

10. Parth Mehta, Dhanashri Gawali, "Conventional versus Vedic mathematical method for Hardware implementation of a multiplier". Department for ETC, Maharashtra Academy of Engg., Alandi(D), Pune, India, 2009 International Conference on Advances in computing and Telecommunication Technologies, pp 641-642.

11. Kang, S., "Accurate simulation of power dissipation in circuits", IEEE Journal of Solid State Circuits, vol. 21, pp 889-891, 1986.

12. Sree Nivas. A, Kayalvizhi. N, Implementation of Power Efficient Vedic Multiplier", International Journal of Computer Applications, vol 43, Issue No.16, April 2012,pp 21-24.